J Electroceram (2012) 28:74–79
DOI 10.1007/s10832-011-9680-5

Characteristics of short-channel amorphous In-Ga-Zn-O thin film transistors and their circuit performance as a load inverter

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Received: 7 October 2011 / Accepted: 26 December 2011 / Published online: 10 January 2012

Abstract The characteristics of amorphous In-Ga-Zn-O (IGZO) thin film transistors (TFTs) and load inverters with a short channel length were studied. The IGZO TFTs showed a mobility value of>5 cm^2/Vs with a V_{th} value of -1.62 V. No degradation of the TFT properties, such as a negative shift of V_{th} or degradation of the subthreshold slope by the short-channel effect, were observed down to a channel length of 2 μm. A load inverter using an IGZO TFT with a gate length of 2 μm and resistor of 1 MΩ was fabricated and characterized, and a voltage gain of 4 was obtained at a V_{DD} value of 10 V. Additionally, the action of a dynamic inverter operating at frequencies of 1 and 10 kHz was characterized. Complete inverter action was obtained at 1 kHz, while an delay time of 0.53 μs was observed at 10 kHz. These promising results indicate that short channel IGZO TFTs are candidate for TFTs in the display industry, including active-matrix organic light-emitting diodes or multi-view three-dimension TV.

Keywords InGaZnO · Oxide thin film transistor · Short channel · Load invertor

1 Introduction

Oxide semiconductors such as indium gallium zinc oxide (IGZO) or hafnium indium zinc oxide (HIZO) have been the subject of intensive research owing to their high potential for use in thin film transistors (TFTs) [1]. Due to their high field-effect mobility (>3 cm^2/Vs) [2] compared to that of amorphous silicon (a-Si) devices (~0.5 cm^2/V s), oxide TFTs are promising switching elements for high-resolution displays, such as ultra-high-definition (2000×4000), large size (> 50 in.), and high frame rate operation (>240 Hz) active-matrix liquid-crystal-display (AMLCD) products. In addition, their amorphous structure can enhance the large area uniformity compared with poly-Si TFTs for AMOLED (active-matrix organic light-emitting diode) displays.

To achieve future AMOLED displays and/or 3-D TV, the TFTs should have a short channel in order to reduce the area, because at least four TFTs are used for the backplane to offset the V_{th} shift during the operation of AMOLEDs. Moreover, for high-resolution UD and non-glass type multi-view 3D displays that do not induce dizziness, a small pixel size is necessary. However, the characteristics of TFTs using a short channel regime have rarely been studied. Most previously reported oxide TFTs, although applied in industry, have large physical dimensions (channel lengths>10 μm) [3, 4]. Furthermore, the majority of the work concerned improvements to the characteristics of the TFTs, such as their structure, channel layer, and reliability, rather than their circuit performance [5, 6]. Previous studies of short-channel oxide TFTs did not report on their circuit performances [7, 8]. Previous studies that did focus on the performance of the circuits, such as inverters or ring oscillators, using oxide TFTs only involved long-channel oxide TFTs [9–11]. Thus, the device and circuit performances capabilities of circuits using short-channel oxide TFTs need to be examined. In this study, we examined the characteristics of short-channel IGZO TFTs and load inverters. TFTs with a channel length of 2~20 μm were fabricated by photo-lithographic

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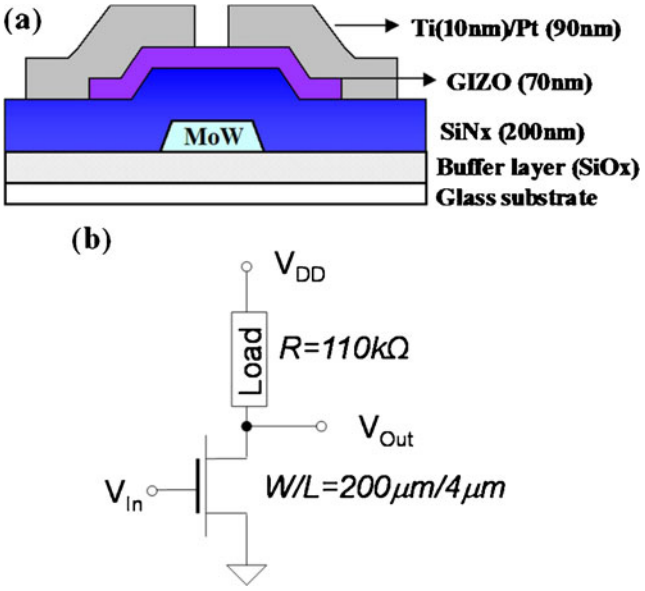

Fig. 1 (**a**) Schematic cross-section diagram of an inverted staggered IGZO TFT, and (**b**) schematic circuit diagram of the inverter setup

patterning. No short-channel effects were observed even with a channel length of 2 μm and a reasonable voltage gain $-(dV_{out}/dV_{in})>4$ was observed from the load inverter

2 Experimental

MoW (150 nm) as a gate metal was deposited and patterned by conventional photolithography on a glass substrate. Then, a 200-nm-thick SiN_x film was grown on the substrate by PE-CVD (plasma enhanced chemical vapor deposition) to act as a gate dielectric. A 70 nm active layer (a- IGZO target : In_2O_3:Ga_2O_3:ZnO=1:1:1 mol%) was deposited by RF sputtering, using a power of 200 W, a working pressure of 5 mTorr, and an O_2/Ar (ratio=0.005) atmosphere at room temperature. The active layer and source/drain (S/D) regions were defined using photolithography and lift-off processes, respectively. The S/D electrodes were formed with electron-beam evaporated Pt (100 nm)/Ti (10 nm) by lift-off processes. Figure 1(a) shows a cross sectional schematic diagram of the inverted staggered a-IGZO TFT structure with a bottom gate and a top contact. To investigate the short-channel effect, the devices with various channel widths/lengths were characterized using a Keithley 4200 semiconductor parameter analyzer. The channel width and length were varied from 20 to 100 μm and from 2 to 20 μm, respectively. To study the operation of the TFT circuits, a load inverter composed of a 110 kΩ resistor and an IGZO TFT were characterized. Figure 1 (b) The threshold voltage (V_T) and saturation filed-effect mobility were extracted in compliance with the gradual channel-approximation model. The dynamic inverter action was also investigated at 1 and 10 kHz in an input voltage range of -10 to +10 V.

3 Results and discussion

Figure 2 (a) and (b) shows TEM images of the IGZO/electrode interface. Although Mo is a widely used interconnect material in AMLCD panels, electrode materials with low resistivity, such as Pt, must be used for fast frame rates (>240 HZ) and large area (>70 in) displays so as to minimize the signal delay over long distances. In addition, given that Pt film does not adhere well to oxides, an adhesion layer commonly of titanium (Ti) is grown prior to the deposition

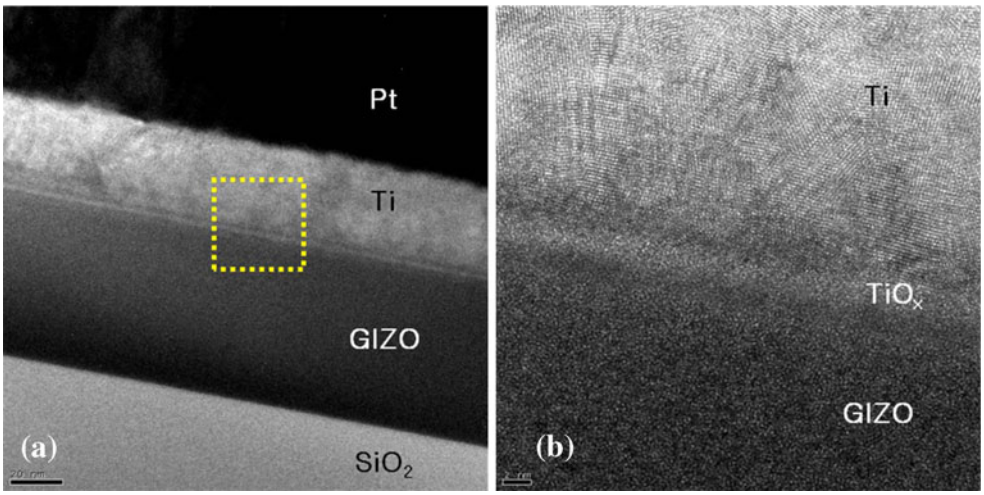

Fig. 2 (**a**) TEM images of the contact region between Ti/Pt source-drain electrodes and an IGZO semiconductor for the devices, and (**b**) magnified image of the interface

of the Pt film. The Ti adhesion layer is used for LCD panel in industry, used in conjunction with Ti/Cu electrode [12, 13]. The interface between the Ti adhesion layer and the underlying IGZO shows the presence of an amorphous TiO_x layer with a thickness of about 3 nm. The formation energy of titanium oxide (968 kJ/mol) is lower than that of indium oxide (909 kJ/mol) and zinc oxide (581 kJ/mol) [14]. It may thus be anticipated that the titanium layer would preferentially consume oxygen from zinc oxide and indium oxide.

The transfer characteristics of the IGZO TFTs with various channel lengths were investigated. Figure 3(a) shows the transfer curves of the IGZO TFTs with a

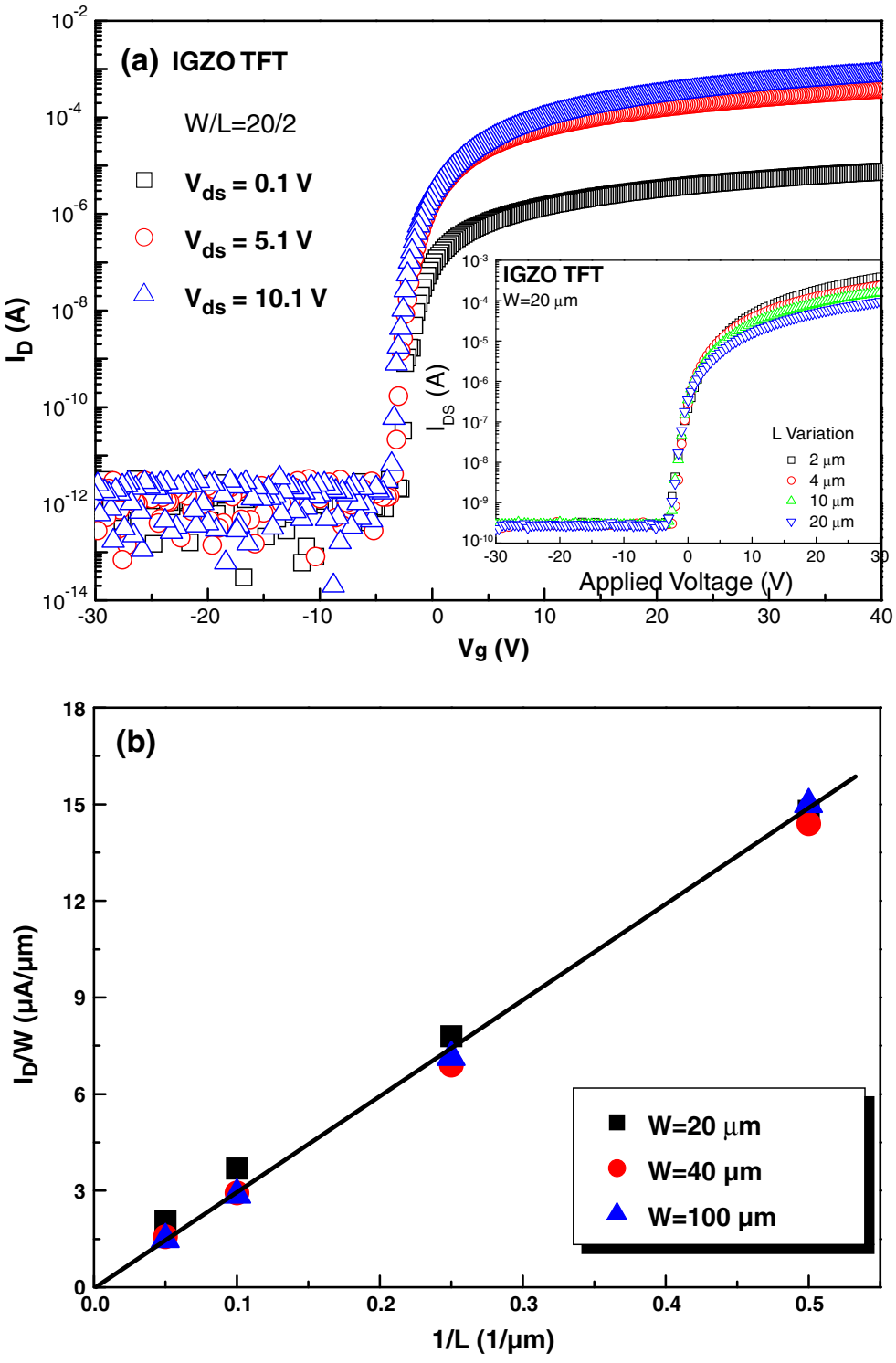

Fig. 3 (**a**) Transfer curves of IGZO TFTs at W/L=20/2 μm under various source/drain voltages. The inset shows transfer curves of various channel lengths (2~20 μm) when V_{sd}=10 V (**b**) The scaling of I_D/W as a function of 1/L for TFTs with various W values. The solid line represents the calculated scaling values

channel length of 2 μm and a width of 20 μm at various gate voltages. The TFTs exhibited an on-to-off ratio of nearly 10^6. In the saturation region, a mobility value of 5.68 cm^2/Vs and V_{th} value of -1.62 V were observed at a V_{ds} value of 10.1 V. The subthreshold swing was estimated to be 180 mV/decade.

These values are comparable to those of previously reported oxide TFTs, as well as IGZO TFTs, even with a short channel length [2, 6, 12]. Also, in contrast to the results reported for short-channel (5 μm) ZnO TFTs, no shift of the transfer curves or degradation of the subthreshold swing were observed upon increasing the source-drain voltage [8]. The inset in Fig. 3(a) shows the transfer curves as a function of various channel lengths. A negative shift of V_{th} was not observed up to a channel length of 2 μm. However, the maximum field-effect mobility of the a- IGZO TFTs decreased from 9.4 to 7.0 cm^2/V s as the channel length decreased from 20 to 6 μm. This mobility reduction may indicate the existence of patristic resistance such as source/drain contact resistance due to non-Ohmic contact or Schottky barrier formation due to the TiO_x interlayer [12, 15]. Figure 3(b) shows the I_d/W value as a function of the inverse of the gate length. Interestingly, the I_d/W value varied almost linearly with 1/L. These two results show that the characteristics of the present IGZO TFTs were dominated by the long channel field effect transistor, which is described by Eq. 1.

$$I_{ds} = \frac{I}{2}\mu C_i \frac{W}{L}(V_g - V_{th})^2 \quad (1)$$

Here, μ is the mobility, C_i is the capacitance per unit area of the gate insulator, and V_g is the gate voltage. From this

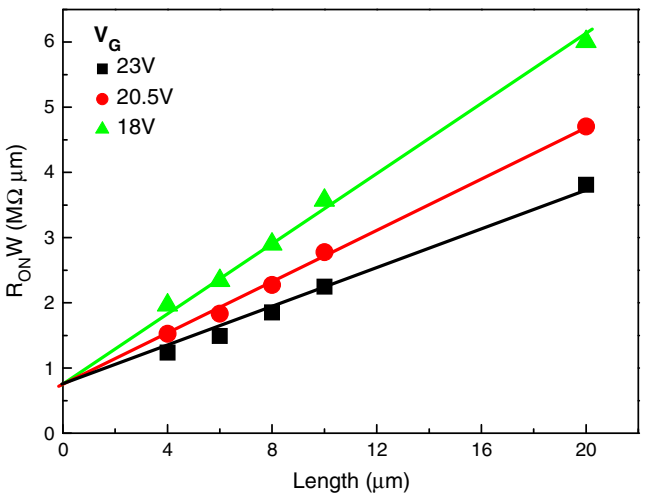

Fig. 4 Plots of the width-normalized total resistance (RonW) vs. the physical channel length of the devices. The plots were generated at different gate voltages. The resistance value at the intersection of the least square fit lines is the total contact resistance

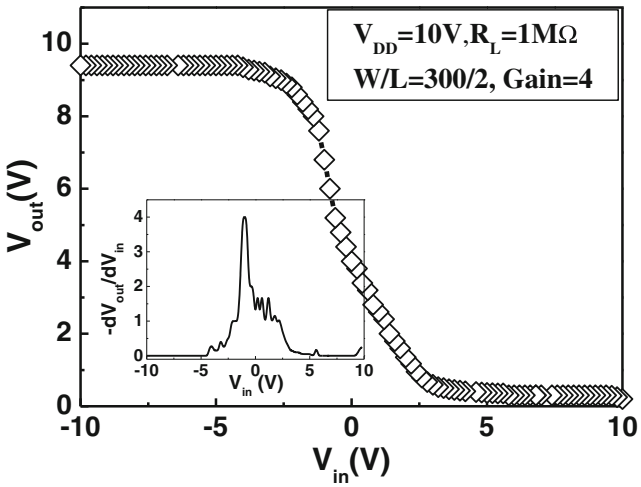

Fig. 5 DC characteristics of the load inverter when L=2 μm and W=100 μm; measured at V_{DD}=10 V. The inset shows a voltage gain $-(dV_{out}/dV_{in})$ of~approximately 4

equation, if the short-channel effect was observed, the I_d/W value as a function of 1/L cannot retain its linear relationship, and degradation of the subthreshold swing in the short

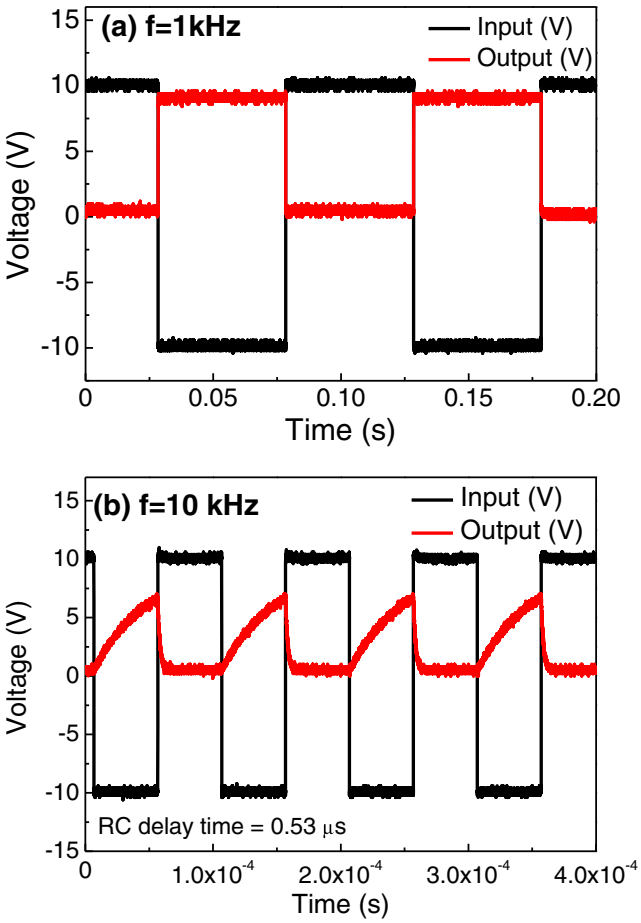

Fig. 6 Dynamic inverter action of an IGZO TFTs when W/L=300/2: (**a**) with a 1 Hz V_{in} signal and (**b**) with a 1 kHz V_{in} signal

channel regime arises (<5 μm at ZnO TFT, and <3 μm at poly Si TFT) [8, 16]. However, our IGZO TFTs did not exhibit any short-channel effects. In a previous study, no short-channel effects were observed for IGZO TFTs with Mo source/drain electrodes, in spite of a channel length of 50 nm corresponding to the short-channel regime, even in the case of metal-oxide-semiconductor field-effect-transistor (MOSFET) devices [7]. In this case, the drain voltage would be consumed upon the penetration of the Schottky barrier and the depletion width would become narrower at the Mo/IGZO contact. However, it is not likely that the interfacial TiO_x layer forms a Shottky barrier between the S/D and the active layer. Generally, TiO_2 is studied as an insulator or conductor such as a gate dielectric [17] or resistive-random-access-memory (RRAM) [18], both of which are dependent with the stoichiometry. In addition, nonstoichiometric TiO_x with a high level of oxygen vacancies had been shown to be generated at the ZnO/Ti interface by oxygen scavengers [19]. Thus, conducting interfacial TiO_x can form.

To investigate the barrier formation of interfacial TiO_x, the contact resistance was measured by transmission line model (TLM) method. The TFT on-resistance (R_{on}) can be defined as the sum of the channel resistance (R_{ch}) and the source-drain contact resistance (R_{sd}) by the following equation:

$$R_{on} = \frac{V_D}{I_D} = R_{ch} + R_{sd} = \frac{L - \Delta L}{\mu_{eff} C_{ox} W (V_G - V_T)} + R_{sd} \quad (2)$$

Here, L is the physical channel length, and the effective length is defined by $L_{eff}=L-\triangle L$. Devices with different physical lengths (L) were selected and the width normalized total resistance ($R_{on}W$) values were computed from the corresponding transfer curves at different gate voltages Fig. 4. In compliance with Eq. 2, the width-normalized contact resistance ($R_{sd}W$) is 75.4 Ωcm, a value comparable to that of previous IGZO TFTs [15, 20]. This resistance value suggests that the interfacial TiO_x barrier was not sufficient for the formation of a high Schottky barrier. This implies that the major contribution to the contact resistance comes from the bulk a-IGZO layer, specifically in how it limits to access to the channel, rather than from the a-IGZO/source (drain) electrode interface with its low contact resistance [21]. Furthermore, this contact resistance may be responsible for a recution of the field-effect mobility with the reduction of the channel length.

Figure 5(a) shows the static behavior of our load inverter at 1 MΩ at a supply voltage (V_{DD}) of 10 V. The maximum output voltage gain $-(dV_{out}/dV_{in})$ was 4, as shown in the inset of Fig. 5. This value is slightly higher than that of an earlier load inverter, which used a long-channel ZnO TFT in spite of its short-channel length [22]. The action of the dynamic inverter was studied using pulsed DC voltage Fig. 6(a) and (b). DC pulsing at an input voltage of 20 V (V_{in}=-10 –and 10 V) was carried out at two different frequencies, 1 and 10 kHz. At 1 kHz, the rising and falling times were nearly identical and clear inverter action was observed. However, at 10 kHz, a small difference in the rising and falling time was observed and the output signal was not square-like. This property was induced by the inevitable RC delay under dynamic operation resulting from the parasitic capacitance in the circuit or TFT structure [23]. In Fig. 6(b), a rising delay time (RC_{rising} time) of about 0.53 μsec can be observed. This delay time is related to the parasitic capacitance (≈300 pF), originating from the source-drain/gate overlap area and from the measurement system. This relatively high parasitic capacitance may be induced during low-frequency operation. Thus, the better dynamic properties would be achieved using low parasitic-capacitance equipment during further investigations. Nevertheless, these dynamic properties were much better than those of a previously reported long-channel ZnO load inverter [22, 23].

4 Conclusion

In this study, we investigated the properties of IGZO TFTs and the characteristics of inverters with a short channel length. A mobility of >5 cm^2/Vs and an on/off ratio as high as 10^7 were achieved for all of the channel lengths and widths investigated. In this study, no short-channel effects, such as a negative shift of V_{th} or degradation of the subthreshold swing, were observed down to a channel length of ~2 μm. The characteristics of load inverters using these short channel IGZO TFTs showed a maximum voltage gain of >4 and a RC delay time of 0.53 μs at 10 kHz. According to the results, short-channel IGZO TFTs with a Ti source/drain are a good candidate for use in the backplane devices of future AMOLEDs and multi-view 3D displays.

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